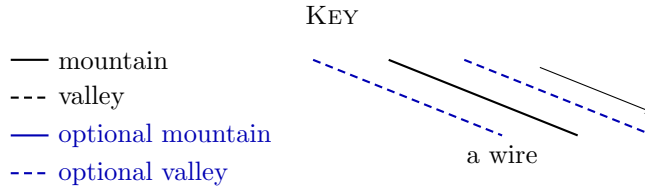


# ORIGAMI LOGIC GADGETS

THOMAS C. HULL AND INNA ZAKHAREVICH



## NOTES

The important gates (OR, AND, NOR, NAND, and NOT) each get a page; each gadget is repeated 4 times, to aid in printing and experimentation. The intersector, twists, and eaters are important if you're trying to construct large patterns (such as Rule 110) but are not necessary for just experimenting with gates independently. They are each repeated twice.

**It is important to remember that none of the creases are bidirectional: each black crease MUST be folded, and each blue crease can either be flat, or folded in the specified direction.**

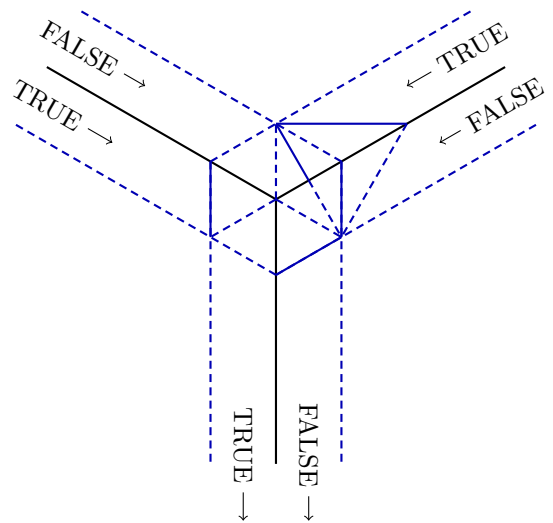
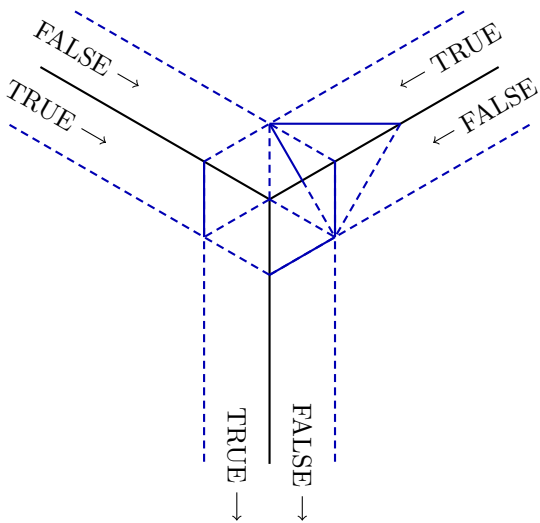
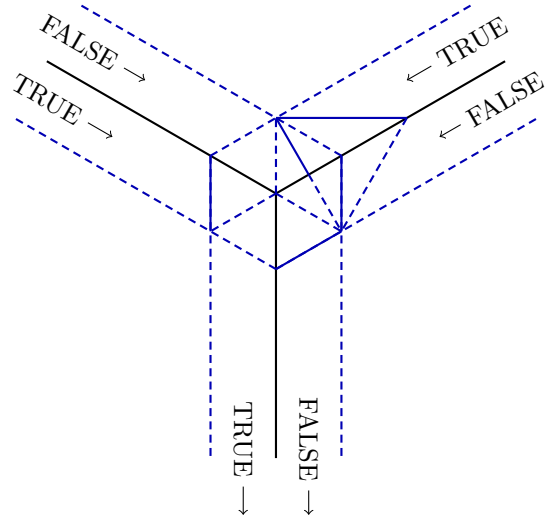
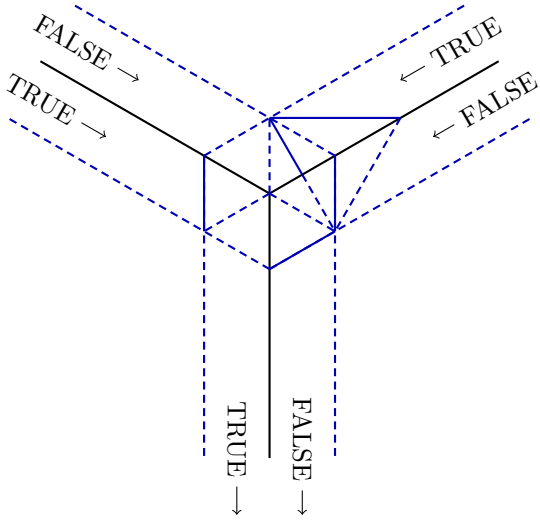
The last page contains the map for how to place gates to make an XOR pattern. If the TRUE side of wires is colored one color and the FALSE side another, a tiling of these should produce a Sierpinski triangle (if the folder is determined enough and the paper is large enough).

If you come up with other gadgets, or just want to show us something you folded, we'd love to see them! In particular, a simpler XOR pattern (or an XOR gadget!) would be very exciting. Email is at [thull1@fandm.edu](mailto:thull1@fandm.edu) or [zakh@math.cornell.edu](mailto:zakh@math.cornell.edu).

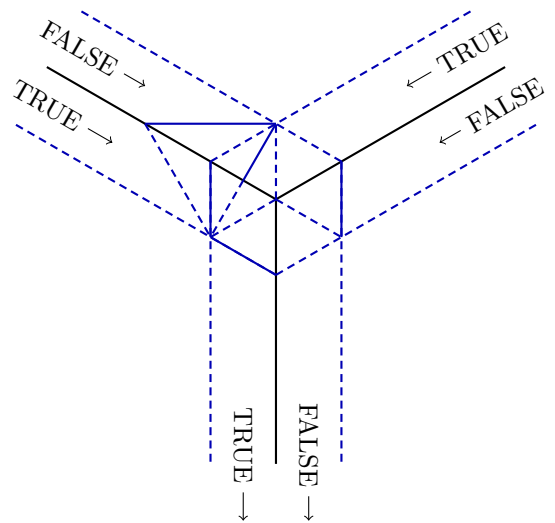
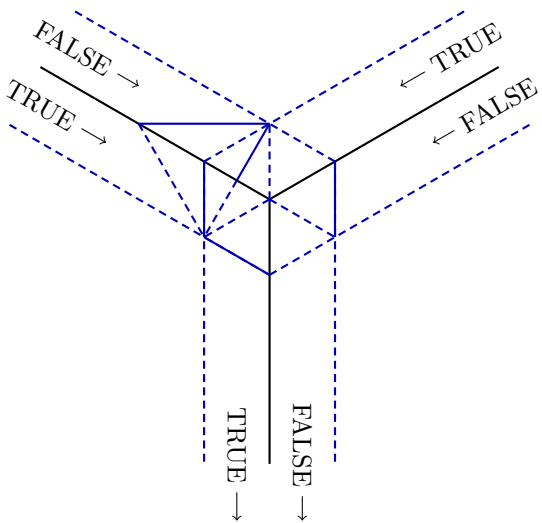
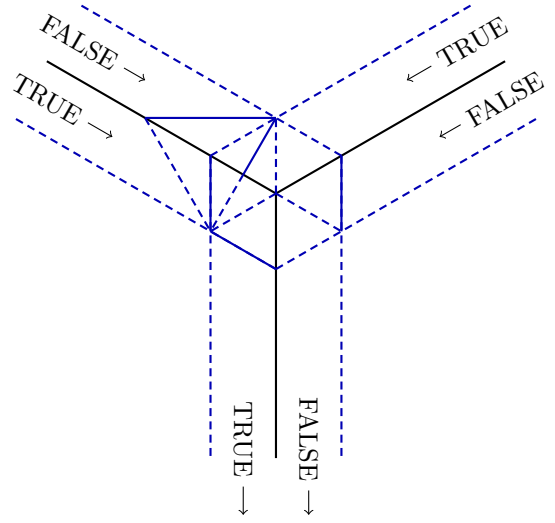
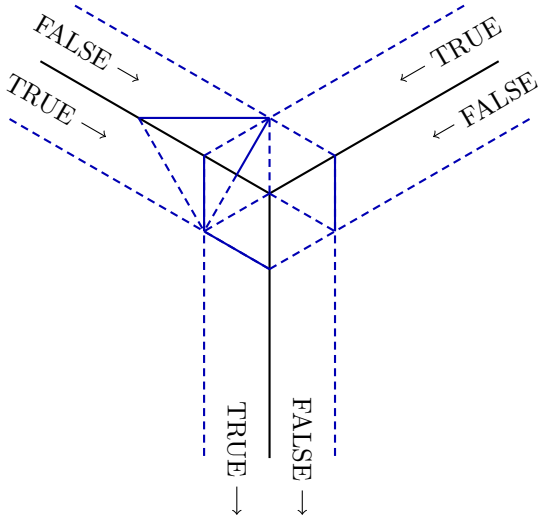
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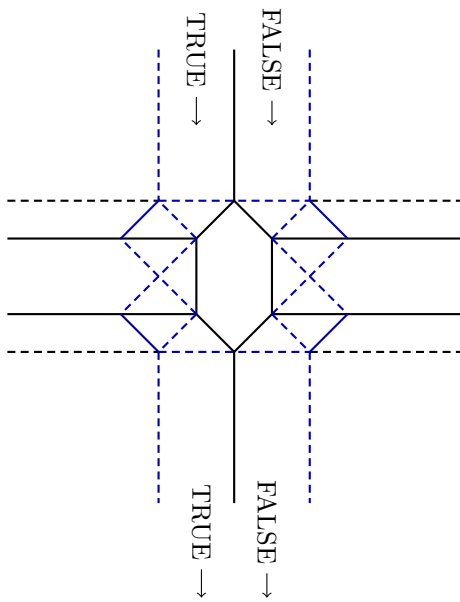
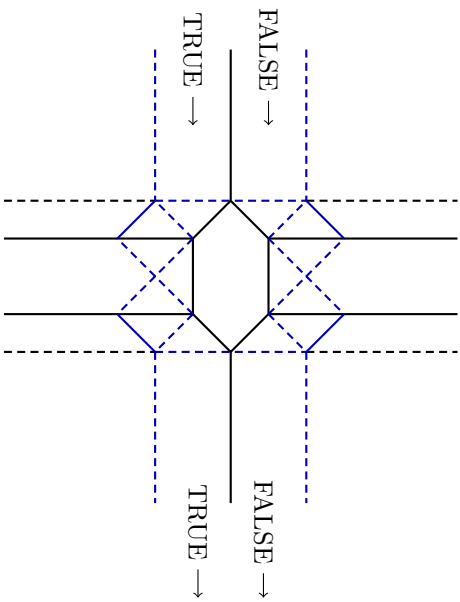
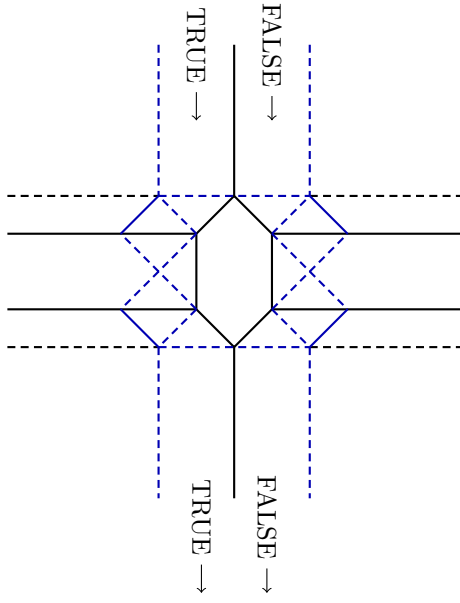
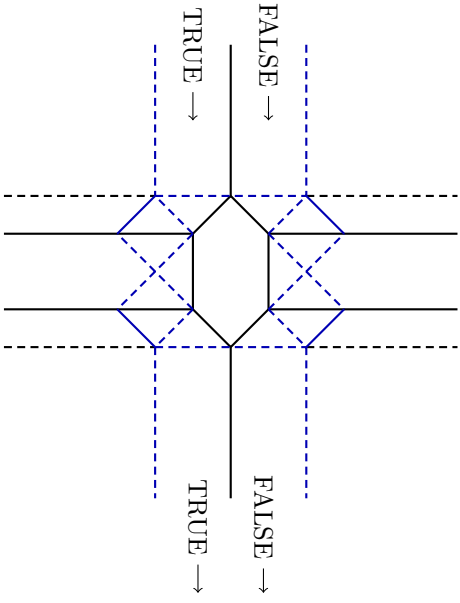
OR



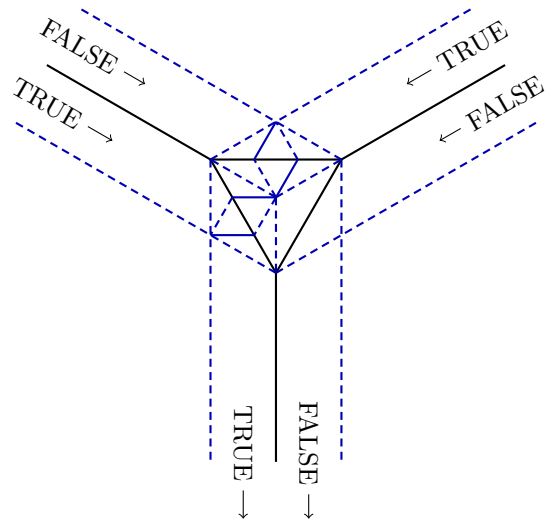
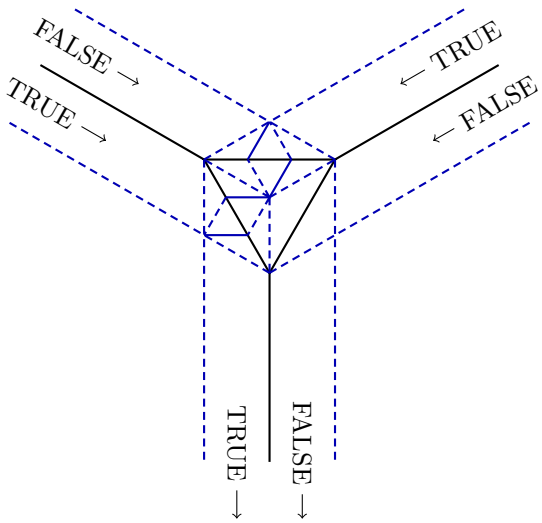
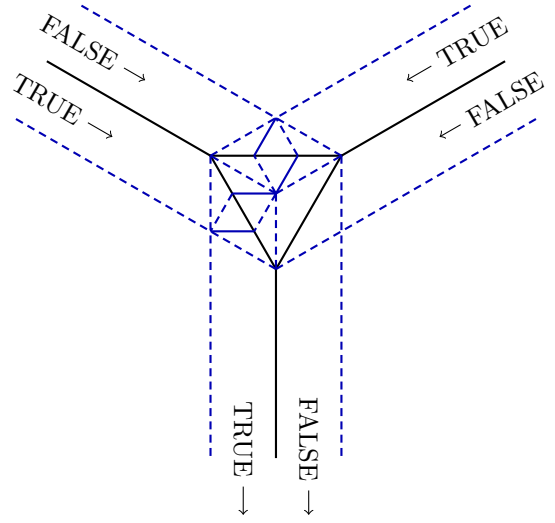
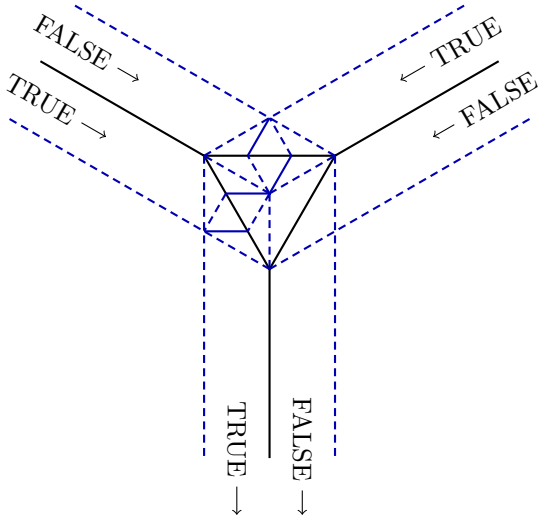
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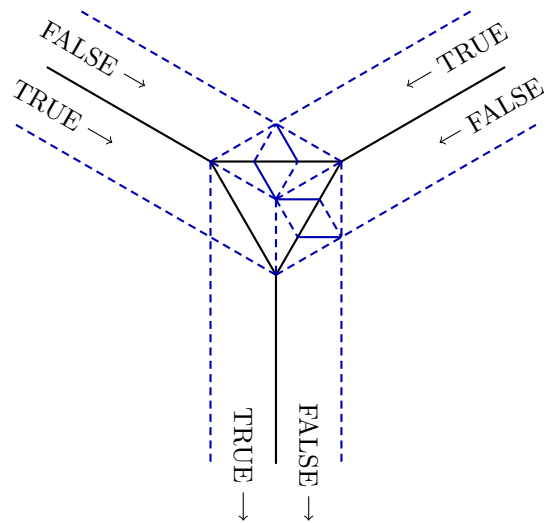
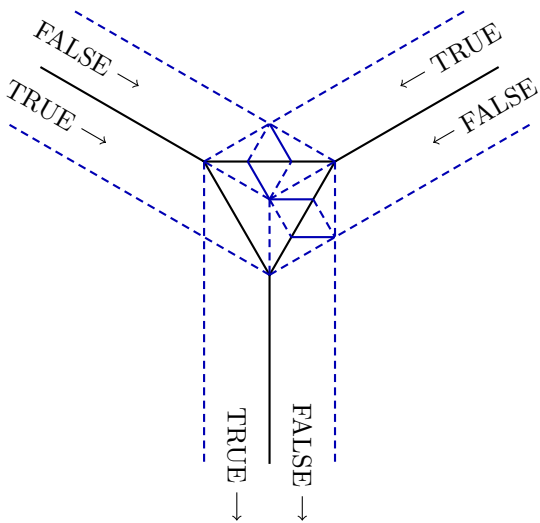
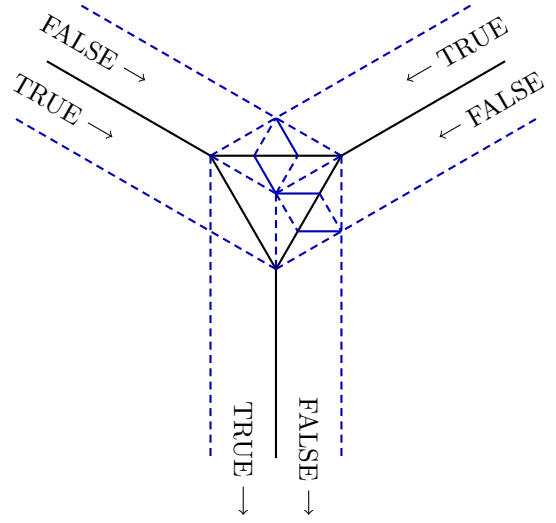
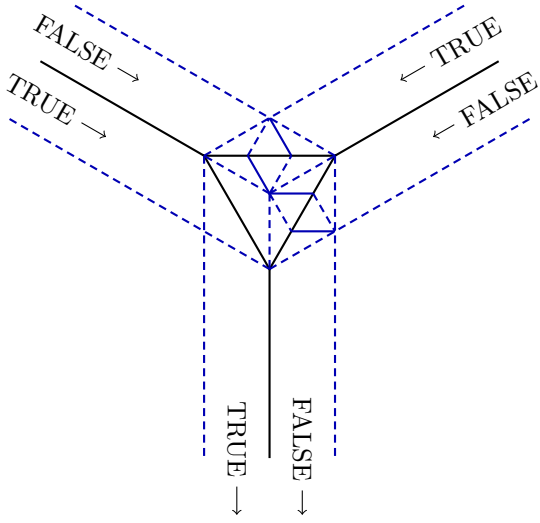
NOT



NOR

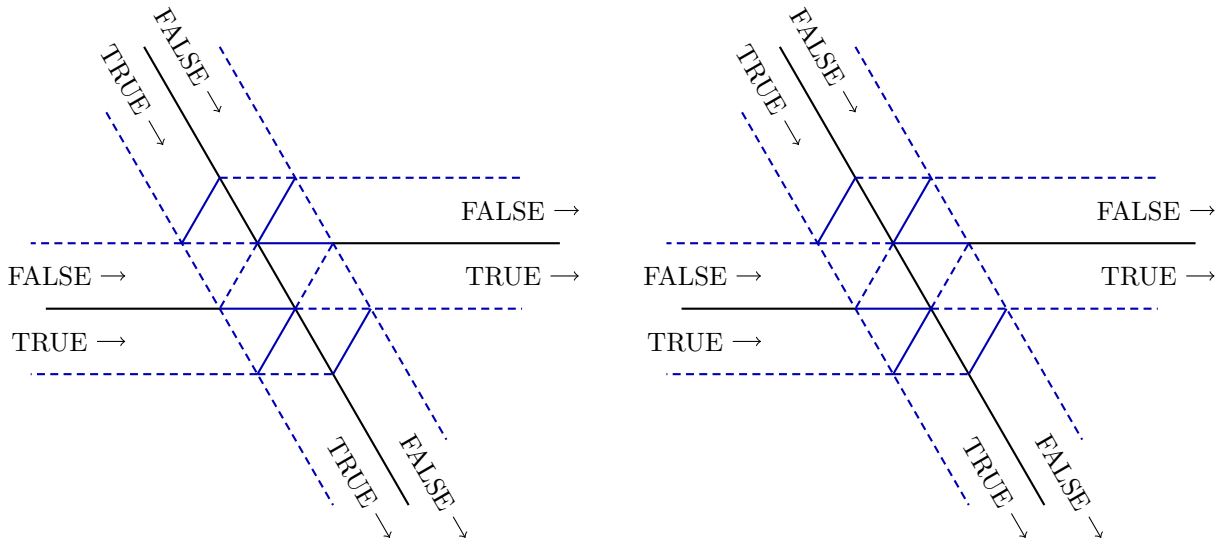


NAND

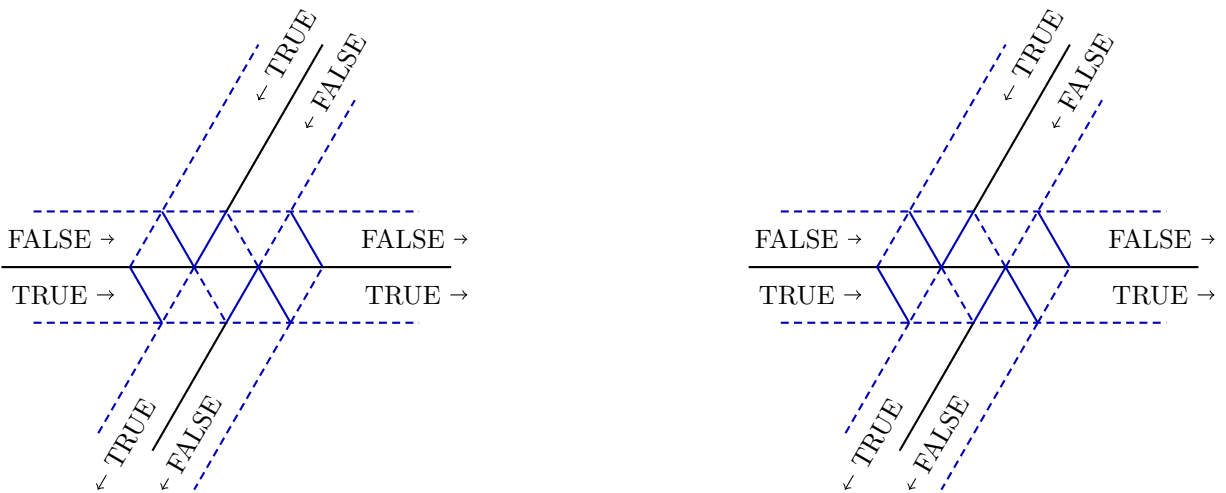


THE INTERSECTORS

$\pi/3$  intersector.

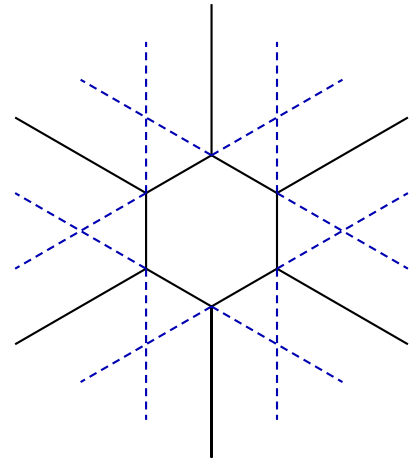
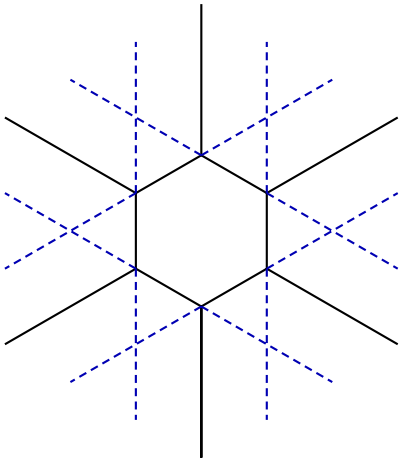


$2\pi/3$  intersector.

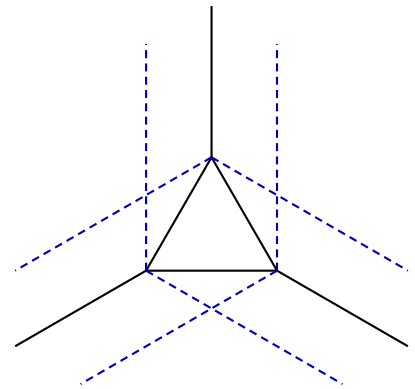
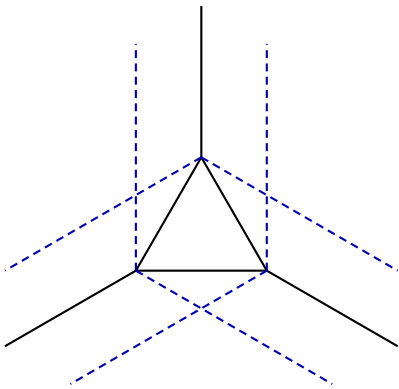


TWISTS

Hexagonal twist.

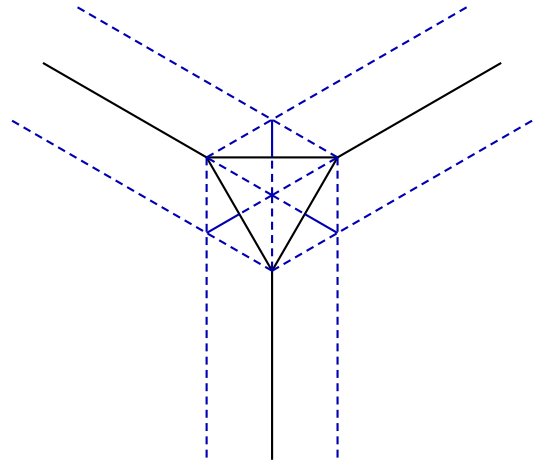
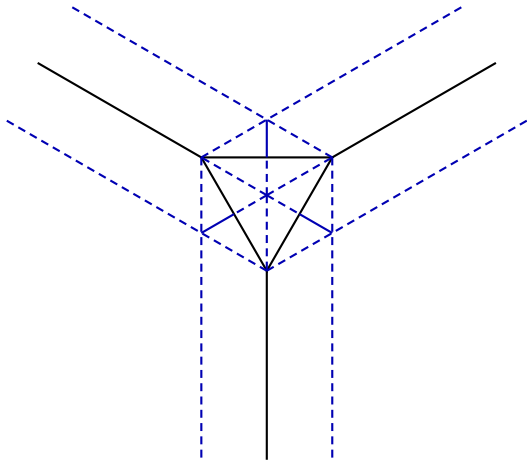


Triangular Twist.



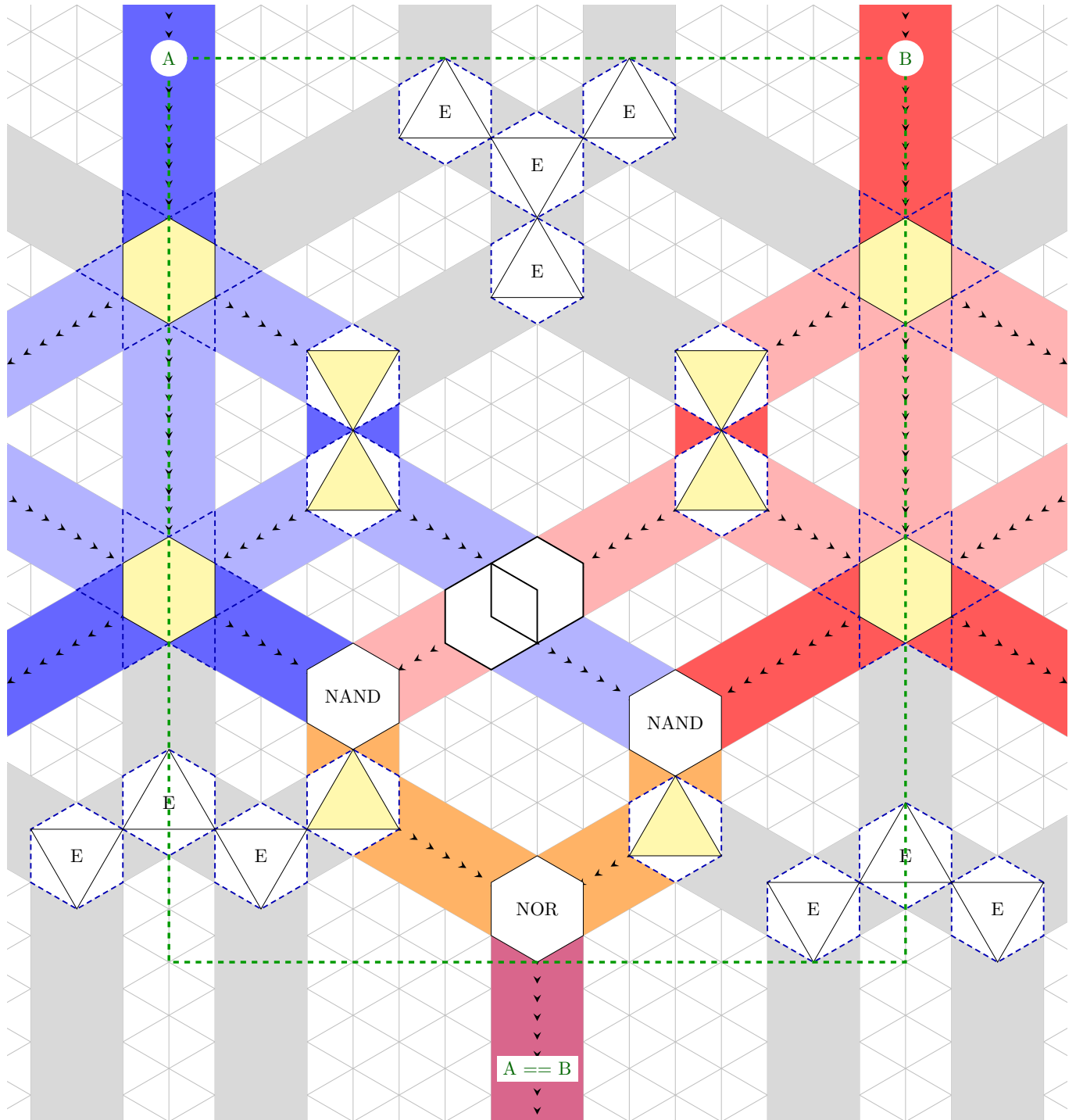


THE EATER



## THE XOR PATTERN

The colored stripes are wires carrying information. The yellow shapes are appropriately-chosen twists. The triangles labeled “E” are eaters; the gates are labeled with their names. To tessellate this is it important to note that the left-hand and right-hand side are not aligned, so adjacent cells need to be reflected (but keeping the gates both NAND). (Since the output is symmetric in  $A$  and  $B$ , the reflection does not affect the output of the cell.)



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