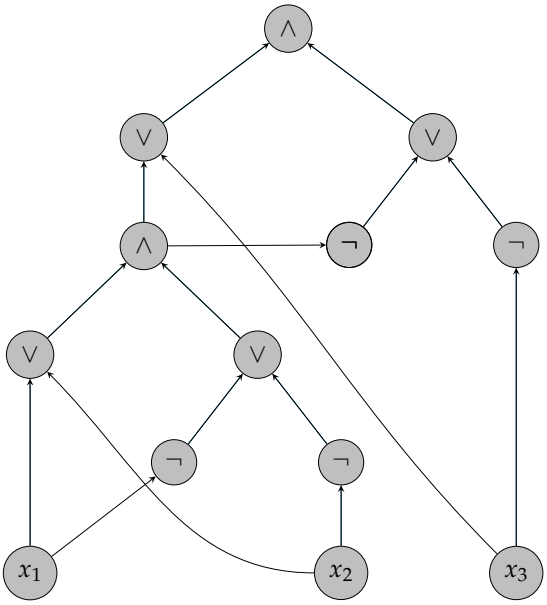
Circuit lower bounds for parity

Undergraduate Math Club
CORNELL UNIVERSITY



NC^1 circuit for computing the parity of three input bits

SPEAKER

Caleb Koch

ABSTRACT

Boolean circuits are a restricted model of computation where one can find many interesting lower bound results. One such result is that, for n large enough, the parity of n bits cannot be computed by constant-depth, polynomial-size circuits with unbounded fan-in. I'll discuss the Razborov-Smolensky proof of this lower bound using the method of approximation after reviewing some requisite circuit complexity.

Please note the unusual schedule – this talk will be on a Wednesday.

SEP 11 at 5:15pm

Malott 532 ⋆ Refreshments